

L Number	Hits	Search Text	DB	Time stamp
-	33204	((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 14:11
-	116	((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 17:15
-	23	(((((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard) and collision) and (concurrent or simultaneous or parallel or synchronous)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 14:09
-	20	((((((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard) and collision) and (concurrent or simultaneous or parallel or synchronous)) and (paramater or variable or constant)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 17:17
-	2	(((((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard) and collision) and database	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 17:17
-	2	((((((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard) and collision) and (concurrent or simultaneous or parallel or synchronous)) and (paramater or variable or constant)) and database	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 17:18
-	23	(((((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and Neuman\$ and harvard) and collision	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:22
-	1476	((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) and ((IC or (integrated adj circuit) or semi?conductor or circuit) or LSI or VLSI) and buffer and collision	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:04
-	531	((simulat\$3 or emulat\$3 or model\$4 or design\$3) same bus) same ((IC or (integrated adj circuit) or semi?conductor or circuit) or LSI or VLSI)) and buffer and collision	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:21
-	1147	collision same bus same (transaction or operation or instruction or function)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:22
-	112	(collision same bus same (transaction or operation or instruction or function)) same (simulat\$3 or emulat\$3 or model\$4 or design\$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:22
-	51	((collision same bus same (transaction or operation or instruction or function)) same (simulat\$3 or emulat\$3 or model\$4 or design\$3)) and (bus same buffer) and (concurrent or simultaneous or parallel or synchronous)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:29
-	3	5907698.uref.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:32
-	1	5907698.pn.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:43
-	1	"5111413".PN.	USPAT	2003/07/10 19:32
-	1	"5461577".PN.	USPAT	2003/07/10 19:32
-	1	"5471398".PN.	USPAT	2003/07/10 19:32

-	1	"5541849".PN.	USPAT	2003/07/10 19:32
-	1	"5761079".PN.	USPAT	2003/07/10 19:32
-	366	collision with bus with (transaction or operation or instruction or function)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:43
-	248	(collision with bus with (transaction or operation or instruction or function)) and (simulat\$3 or emulat\$3 or model\$4 or design\$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:44
-	17	(collision with bus with (transaction or operation or instruction or function)) same (simulat\$3 or emulat\$3 or model\$4 or design\$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 19:45
-	1	5724504.pn.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/10 20:44
-	1627	bus adj (design\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/11 14:07
-	216	(bus adj (design\$3)) and collision	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/11 14:07
-	173	((bus adj (design\$3)) and collision) and (buffer or stack or FIFO)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/11 14:08
-	152	((((bus adj (design\$3)) and collision) and (buffer or stack or FIFO)) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 14:08
-	148	((((bus adj (design\$3)) and collision) and (buffer or stack or FIFO)) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and (concurrent or simultaneous or parallel or synchronous)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 14:11
-	104	(((((bus adj (design\$3)) and collision) and (buffer or stack or FIFO)) and (IC or (integrated adj circuit) or semi?conductor or circuit or LSI or VLSI)) and (concurrent or simultaneous or parallel or synchronous)) and (simulat\$3 or emulat\$3 or model\$4)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 15:12
-	13191	bus same (simulat\$3 or emulat\$3 or model\$4)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 16:24
-	2358	bus same (simulat\$3 or emulat\$3 or model\$4) same (collision or block\$2)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/07/11 16:25

Welcome
United States Patent and Trademark Office

[Help](#)
[FAQ](#)
[Terms](#)
[IEEE](#)
[Quick Links](#)
[» Search Results](#)

[Peer Review](#)

Welcome to IEEE Xplore®

☐ Home
☐ What Can I Access?
☐ Log-out

Tables of Contents

☐ Journals & Magazines
☐ Conference Proceedings
☐ Standards

Search

☐ By Author
☐ Basic
☐ Advanced

Member Services

☐ Join IEEE
☐ Establish IEEE Web Account
☐ Access the IEEE Member Digital Library
 Print Format

Your search matched **2164** of **951805** documents.

A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.

You may refine your search by editing the current search expression or entering a new one in the text box.

Then click **Search Again**.

(simulat*) <and> (bus)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

16 PPMB: a partial-multiple-bus multiprocessor architecture with improved cost-effectiveness
Jiang, H.; Smith, K.C.;
Computers, IEEE Transactions on , Volume: 41 Issue: 3 , March 1992
Page(s): 361 -366

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) **IEEE JNL**

17 An easy-to-use approach for practical bus-based system design
Chung-Ho Chen; Feng-Fu Lin;
Computers, IEEE Transactions on , Volume: 48 Issue: 8 , Aug. 1999
Page(s): 780 -793

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) **IEEE JNL**

18 32-bit PI-bus versus 32-bit Futurebus+ performance comparison
Emmitt, J.;
Aerospace and Electronics Conference, 1993. NAECON 1993., Proceedings of the IEEE 1993 National , 24-28 May 1993
Page(s): 157 -164 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(572 KB\)\]](#) **IEEE CNF**

19 A high-speed, byte-serial, multiple-bus interconnection network

Armstrong, W.J.; Pohm, A.V.; Davis, J.A.;
Communications, Computers and Signal Processing, 1989.
Conference Proceeding., IEEE Pacific Rim Conference on , 1-2 June
1989
Page(s): 64 -69

[\[Abstract\]](#) [\[PDF Full-Text \(440 KB\)\]](#) [IEEE CNF](#)

20 Performance analysis of asynchronous hierarchical-bus multiprocessor systems using closed queuing network models

Mahmud, S.M.;

Circuits and Systems, 1990., IEEE International Symposium on , 1-3
May 1990

Page(s): 2689 -2692 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) [IEEE CNF](#)

21 Optimal design of megabyte second-level caches for minimizing bus traffic in shared-memory shared-bus multiprocessors

Yen-Jen Oyang; Le-Chun Wu;

System Sciences, 1992. Proceedings of the Twenty-Fifth Hawaii
International Conference on , Volume: i , 7-10 Jan. 1992

Page(s): 467 -475 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(460 KB\)\]](#) [IEEE CNF](#)

22 Performance model for a prioritized multiple-bus multiprocessor system

Kurian, L.; Yu-Cheng Liu;

Parallel and Distributed Processing, 1994. Proceedings. Sixth IEEE
Symposium on , 26-29 Oct. 1994

Page(s): 577 -584

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) [IEEE CNF](#)

23 Modeling and evaluation of adaptive bus-preemption control with and without AVL systems

Gang-Len Chang; Vasudevan, M.; Chih-Chiang Su;

Vehicle Navigation and Information Systems Conference, 1995.
Proceedings. In conjunction with the Pacific Rim TransTech
Conference. 6th International VNIS. 'A Ride into the Future' , 30
July-2 Aug. 1995

Page(s): 305 -316

[\[Abstract\]](#) [\[PDF Full-Text \(832 KB\)\]](#) [IEEE CNF](#)

24 Testing and evaluation of batteries for a fuel cell powered hybrid bus

Miller, J.F.; Webster, C.E.; Tummillo, A.F.; DeLuca, W.H.;
Energy Conversion Engineering Conference, 1997. IECEC-97.
Proceedings of the 32nd Intersociety , 27 July-1 Aug. 1997
Page(s): 894 -898 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) [IEEE CNF](#)

25 Network simulations of a general class of partial-connection multiple-bus systems

Tu, H.-Y.; Hawkes, L.W.;
Modeling, Analysis and Simulation of Computer and Telecommunication Systems, 1999. Proceedings. 7th International Symposium on , 24-28 Oct. 1999
Page(s): 120 -127

[\[Abstract\]](#) [\[PDF Full-Text \(124 KB\)\]](#) [IEEE CNF](#)

26 Fast computations on a low-cost DSP-based shared-memory multiprocessor system

Christou, C.S.;
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 1 , 17-20 Dec. 2000
Page(s): 189 -192 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) [IEEE CNF](#)

27 Reducing power bus impedance at resonance with lossy components

Zeeff, T.M.; Hubing, T.H.;
Electrical Performance of Electronic Packaging, 2001 , 29-31 Oct. 2001
Page(s): 61 -64

[\[Abstract\]](#) [\[PDF Full-Text \(266 KB\)\]](#) [IEEE CNF](#)

28 Computer modeling and simulation of the Optoelectronic Technology Consortium (OETC) optical bus

Whitlock, B.K.; Pepeljugin, P.K.; Kuchta, D.M.; Crow, J.D.; Kang, S.-M.;
Selected Areas in Communications, IEEE Journal on , Volume: 15 Issue: 4 , May 1997
Page(s): 717 -730

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) **IEEE JNL**

29 On the nature and inadequacies of transport timing delay constructs in VHDL descriptions

Walker, P.A.; Ghosh, S.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 Issue: 8 , Aug. 1997

Page(s): 894 -915

[\[Abstract\]](#) [\[PDF Full-Text \(472 KB\)\]](#) **IEEE JNL**

30 A bus-monitoring model for MPEG video decoder design

Nam Ling; Jui-Hua Li;

Consumer Electronics, IEEE Transactions on , Volume: 43 Issue: 3 , Aug. 1997

Page(s): 526 -530

[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) **IEEE JNL**

[\[Prev\]](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [12](#) [13](#) [14](#) [15](#) [16](#) [17](#) [18](#) [19](#) [20](#) [21](#) [22](#) [23](#) [24](#)
[25](#) [26](#) [27](#) [28](#) [29](#) [30](#) [31](#) [32](#) [33](#) [34](#) [\[Next\]](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved

**IEEE Xplore®**
RELEASE 1.5Welcome
United States Patent and Trademark Office[Help](#) [FAQ](#) [Terms](#) [IEEE](#) [Quick Links](#)» [Search Results](#)[Peer Review](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

Print Format

Your search matched **2** of **951805** documents.A maximum of **2** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.

You may refine your search by editing the current search expression or entering a new one in the text box.

Then click **Search Again**.**Results:**Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 A novel reduced swing CMOS bus interface circuit for high speed low power VLSI systems***Golshan, R.; Haroun, B.;*

Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on , Volume: 4 , 30 May-2 June 1994

Page(s): 351 -354 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) **IEEE CNF****2 Steady-state and transient ampacity of bus bar***Coneybeer, R.T.; Black, W.Z.; Bush, R.A.;*

Power Delivery, IEEE Transactions on , Volume: 9 Issue: 4 , Oct. 1994

Page(s): 1822 -1829

[\[Abstract\]](#) [\[PDF Full-Text \(664 KB\)\]](#) **IEEE JNL**

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved